Pentium® Pro, Pentium II, Pentium III, Pentium 4, and Itanium® processors. N-pumping means that N sets of data are transferred per clock cycle, generally by using phase synchronization rather than multi-level signaling.

[0030] As shown, during the first full cycle of the CLK clock signal (from **90** to **92**), eight data bits (in DATA# signal boxes **0** through **7**) are transferred per data wire. In one mode, this is accomplished by latching the data in response to rising and falling edges of four distinct strobe signals STROBE**04**, STROBE**15**, STROBE**26**, and STROBE**37**. The data lines are coupled to latches (BANK**0**); for ease of illustration, the data lines DATA#[31:0] are drawn as though touching only the first latch (latch **0**), but the reader will appreciate that they are connected to the other latches as well. The number of latches in the bank corresponds to the number of "pumps" per clock cycle; the example given is "eight-pumped" and thus has eight latches (0 through 7 in BANK**0**). The strobe signals are coupled to respective individual latches. In the mode in which both the rising and falling edges are used as latch triggers, the number of strobe signals is half the number of latches, and each strobe signal is coupled to two latches, one of which has an inverted input. In order to equalize the duty cycle of the strobe, it is desirable that its two latches be equally spaced within the set of latches in the bank (such as latches **0** and **4**, or latches **2** and **6**).

[0031] The panel controller drives the data wires at a higher frequency than the clock signal, and the strobe signals are phase-synchronized to match this frequency multiplication. In one mode, the latch signals are not transmitted as wires between the panel controller and the panel, but are generated within the panel itself, such as within the display sequencer by phase-locked loop or other means.

[0032] One reason why the system designer may wish to N-pump the data bus is that, in some cases, the technology of the panel may not allow the various logic devices of the panel to be directly clocked at a frequency sufficient to meet the data transfer rate requirements of the panel. In some panels, it may be desirable to fab the logic directly on the glass; this may result in a maximum logic frequency of 8 MHz, for example. Another solution to this problem is simply to increase the number of data wires, but this drives up the cost and complexity of the display and the display controller. The skilled artisan will understand how to trade off wire count against N-pumping to meet the needs of the application at hand, within the teachings of this patent.

[0033] The N-pumping may work in one direction only, in some embodiments; the configuration data may be provided to the panel controller at the CLK clock rate, or perhaps even some fraction of that frequency.

[0034] **FIG. 6** illustrates a further improvement which may be present in some embodiments of the invention. In order to provide improved buffering, two banks of data latches (BANK**0** and BANK**1**) may be provided, and operates in ping-pong fashion in response to an enable signal (ENABLE, inverted at one bank), as is known in the art. While one bank is filling, the other, already-filled bank is being read and its data are being consumed for display on the panel. A multiplexor (MUX) also responds to the enable signal to select the already-filled bank for reading to output to the panel.

[0035] Parameters

[0036] Table 2 illustrates one embodiment of encoding the Resolution parameter:

TABLE 2

Resolution	
0000	160 × 160
0001	320 × 240 (QVGA)
0010	320 × 320
0011	640 × 480 (VGA)
0100	800 × 600 (SVGA)
0101	1024 × 768 (XGA)
0110	1280 × 1024
0111	1600 × 1200 (UXGA)
1000	1920 × 1080 (HDTV)
1001	3640 × 2048
1010 and up	reserved

[0037] Table 3 illustrates one embodiment of encoding the Data Bus Width parameter:

TABLE 3

Data Bus Width	
000	2-bit data bus
001	4-bit data bus
010	8-bit data bus
011	16-bit data bus
100	32-bit data bus
101	64-bit data bus
110	reserved
111	reserved

[0038] Table 4 illustrates one embodiment of encoding the Display Technology parameter:

TABLE 4

Display Technology	
000	CRT
001	LCD
010	OLED
011	plasma
100	reserved
101	reserved
110	reserved
111	reserved

[0039] Table 5 illustrates one embodiment of encoding the Gray Scale Support parameter:

TABLE 5

Gray Scale Support	
00	reserved
01	8-level gray scale (three bits)
10	16-level gray scale (four bits)
11	256-level gray scale (eight bits)